Exh. 5, d3

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BY FAX - 11 PAGES

Re: TI-25833

Gentlemenl:

Enclosed is a first draft of a patent application for your subject inventon which I have prepared from your disclosure and our discussions.

Please review the draft and advise me of any changes and/or additions which may be required. Also, please advise me if you have come up with some way of defining the distance between traces which can be related to a specific solder ball size that can be defined in this application of some other manner of defining this distance. Please fax your remarks to me at (202) 414-4048, preferably by marking up a copy of the attached draft.

Very truly yours,

Jay M. Cantor

JMC:a
Enclosures

P.S. Nick, please fax a copy to Bill Stearns at (972) 234-0257. I am having difficulty at the moment since I am in California.

Jay

OPTIMIZED CIRCUIT DESIGN LAYOUT FOR HIGH PERFORMANCE BALL GRID ARRAY PACKAGES

CROSS REFERENCE TO RELATED APPLICATIONS

09/046,062

This application is related to Serial No. (TI-22215), the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

This invention relates to a method of laying out traces on a substrate and the layout for connection of a semiconductor chip to a printed wiring board and the like.

BRIEF DESCRIPTION OF THE PRIOR ART

Semiconductor integrated circuits are formed in semiconductor chips which contain the electrical circuits. Bond pads are generally disposed on the chip with the chip being mounted within a package and the bond pads being connected by wires to lead frame fingers or the like which extend externally of the chip. The package is generally secured to a printed wiring board with the lead frame fingers or the like connected to bonding regions on the printed wiring board. The package as well as the electrically

conductive members which transfer the signals from the chip to the printed wiring board adds to the undesirable loads (i.e., inductances, noise, crosstalk, etc.) which the chip may see with these undesirable loads increasing with increase in chip operating frequency.

A typical package includes a substrate having a depression which contains a chip within the depression. Bond wires couple bond pads on the chip to individual copper traces on the substrate, the copper traces each extending to an electrically conductive aperture or via which extends through the substrate to a solder ball. The vias are formed in a matrix array having plural rows and columns of vias which are located adjacent one or more of the sides defining the depression. The solder ball is soldered to a terminal on a printed wiring board in standard manner as discussed in the above noted copending application to make the connection from the chip to the printed wiring board terminal.

The copper traces as well as the bond wires, electrically conductive regions in the vias and surrounding wiring and packaging add additional circuitry to the electrical circuit which bring to the circuit additional resistances, inductances and capacitances. The layout of the circuitry and especially the layout of the traces materially affects the performance of the chip, this being particularly material in the case of differential wiring pairs wherein pairs of wires carry the same or similar signals but are out of phase with each other. It is therefore apparent that a

layout is highly desirable which minimizes the above noted problems of the prior art.

SUMMARY OF THE INVENTION

In accordance with the present invention, the above described problems of the prior art are minimized.

Briefly, the path traversed by each trace of each differential wiring pair is adjusted to have a pitch or distance therebetween substantially equal to or less than the diameter of the solder ball, to be parallel to each for the maximum possible distance, to each be as close as possible to the same length and to have the same geometry to the closest extent possible. The diameter of the solder ball is set by the industry for the size of the package being used and varies, depending upon package size. In other words, it is a requirement that the parallel positioning of the trace portion of each differential wiring pair be maximized to the greatest possible extent and that the trace lengths be equalized to the greatest possible extent. The quality of the differential pairs is dependent upon each of (1) the degree of parallelism, (2) equality of length and (3) identity of geometry between the two traces forming the differential pair. It is also necessary that each trace of the differential pair be equally spaced from the ground plane.

In the present state of the art, it is possible to provide at most two signal traces between a pair of adjacent columns. In order to meet the above criteria, it has been found that the above described maximization is obtained by connecting pairs in the manner 1-2, 1-2 and 3-3. This means that, given a pair of adjacent columns, a first pair of traces will be connected to rows 1 and 2

of a first column with the trace connected row 2 travelling between the columns, a second pair of traces will be connected to rows 1 and 2 of the adjacent column with the trace connected to row 2 extending between the second and third column and a third pair of traces which pass between the first and second columns and are connected to the third row in each of these columns. In the event more than two traces can be passed between a pair of adjacent rows, the above manner of connection would be altered as is apparent.

It should be understood that, though the above described circuit has been laid out to accommodate differential pairs, each trace of each differential pair can be used to accommodate other types of signals.

Advantages of the layout in accordance with the present invention are improved electrical performance, suitability for high frequency applications and flexibility to use nearly all signal traces as differential pairs or single ended lines. Crosstalk is also substantially reduced.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGURE 1 is a schematic diagram of a typical package which can be used in accordance with the prior art as well as in accordance with the present invention;

FIGURE 2 is a cross sectional view of a portion of the package of FIGURE 1 connected to a printed wiring board;

FIGURE 3 is a schematic diagram of a layout in accordance with the present invention; and

FIGURE 4 is a preferred layout using three rows of vias for connection to the chip and a pair of traces between each pair of columns of vias.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to FIGURE 1, there is shown a typical package which can be used in accordance with the prior art as well as in accordance with the present invention. The package is shown with the encapsulation removed and includes a substrate 1 having a depression 3 which contains a chip 5. Bond wires 7 couple bond pads 8 on the chip 5 to individual copper trace 9 on the substrate, the copper traces each extending to an electrically conductive aperture or via 11 which extends through the substrate to a solder ball 13 as shown in FIGURE 2. The vias 11 are formed in a matrix array, there being plural rows and columns of vias which can be located adjacent one or more of the sides defining the depression 3. The solder ball 13 is soldered to a terminal 15 on the printed wiring board 17 in standard manner is discussed in the above noted copending application to make the connection from the chip 5 to the printed wiring board terminal. While the traces 9 are shown on only one layer, it should be understood that there can be plural layers of traces separated by and electrically insulating layer with vias extending from the top layer of the substrate to the lower layer which contain the traces with all connections from the chip to the substrate preferably being made at the topmost level (though it is contemplated that connections can be made directly to a lower layer from the chip).

The copper trace 9 as well as the bond wires 7, electrically conductive region in the via 11 and surrounding wiring add additional circuitry to the electrical circuit which bring to the

circuit additional resistances, inductances and capacitances. The layout of the circuitry and especially the traces 9 materially affect the performance of the chip, this being particularly material in the case of differential wiring pairs wherein pairs of wires carry the same or similar signals but are out of phase with each other. In accordance with the present invention, the path traversed by each trace 9 of each differential wiring pair is adjusted to have a pitch or distance therebetween from trace center line to trace center line of up to the diameter one solder ball 13, to be parallel to each for the maximum possible distance, to each be as close as possible to the same length and to have the same geometry to the closest extent possible. The diameter of the solder ball is set by the industry for the size of the package being used and varies, depending upon package size. In other words, it is a requirement that the parallel positioning of the trace portion of each differential wiring pair be maximized to the greatest possible extent and that the trace lengths be equalized to the greatest possible extent. The quality of the differential pairs is dependent upon each of (1) the degree of parallelism, (2) equality of length and (3) identity of geometry between the two traces forming the differential pair. It is also necessary that each trace of the differential pair be equally spaced from the ground plane. This is shown in FIGURES 3 and 4 wherein differential pairs are shown encircled.

In the present state of the art, it is possible to provide at most three signal traces between a pair of adjacent rows. In order

to meet the above criteria, it has been found that the above described maximization is obtained by connecting pairs in the manner 1-2, 1-2 and 3-3 as shown in FIGURES 3 and 4. In the event more or less than three traces can be or are passed between a pair of adjacent rows, the above manner of connection would be altered as is apparent.

It should be understood that, though the above described circuit has been laid out to accommodate differential pairs, each trace of each differential pair can be used to accommodate other types of signals.

Though the invention has been described with respect to a specific preferred embodiment thereof, many variations and modifications will immediately become apparent to those skilled in the art. It is therefore the intention that the appended claims be interpreted as broadly as possible in view of the prior art to include all such variations and modifications.

CLAIMS

1. A method of laying out traces for connection of bond pads of a semiconductor chip to a printed wiring board or the like which comprises the steps of:

(a) providing a substrate having top and bottom surfaces with a plurality of rows and columns of vias extending therethrough from said top surface to said bottom surface and having a solder ball secured at said bottom surface to each said via; and

(b) providing a plurality of pairs of traces on said top surface, each trace of each of said pairs traces extending to a different one of said vias and extending to vias on a plurality of said rows and columns, each of traces of each of said pair being spaced from the other trace of said pair by up to the diameter of said solder ball, being maximized for identity in length and being maximized for parallelism.

2. The method of claim 1 wherein each of said traces of said pair is further maximized for identity in geometry.

3. The method of claim 1 further comprising the step of applying a differential signal pair to at least one of a said pair of traces.

4. The method of claim 2 further comprising the step of applying a differential signal pair to at least one of a said pair of traces.

5. The method of claim 1 further including the step of providing a further surface between said top and bottom surfaces insulated from said top and bottom surfaces, a plurality of said traces being disposed on said further surface.

6. The method of claim 2 further including the step of providing a further surface between said top and bottom surfaces insulated from said top and bottom surfaces, a plurality of said traces being disposed on said further surface.

7. The method of claim 3 further including the step of providing a further surface between said top and bottom surfaces insulated from said top and bottom surfaces, a plurality of said traces being disposed on said further surface.

8. The method of claim 4 further including the step of providing a further surface between said top and bottom surfaces insulated from said top and bottom surfaces, a plurality of said traces being disposed on said further surface.

9. A layout of traces for connection of bond pads of a semiconductor chip to a printed wiring board or the like which comprises:

(a) a substrate having top and bottom surfaces with a plurality of rows and columns of vias extending therethrough from said top surface to said bottom surface and having a solder ball secured at said bottom surface to each said via; and

(b) a plurality of pairs of traces on said top surface, each trace of each of said pairs traces extending to a different one of said vias and extending to vias on a plurality of said rows and columns, each of traces of each of said pair being spaced from the other trace of said pair by up to the diameter of said solder ball, being maximized for identity in length and being maximized for parallelism.

10. The layout of claim 9 wherein each of said traces of said pair is further maximized for identity in geometry.

11. The layout of claim 9 further including means for applying a differential signal pair to at least one of a said pair of traces.

12. The layout of claim 10 further including means for applying a differential signal pair to at least one of a said pair of traces.

13. The layout of claim 9 further including a further surface between said top and bottom surfaces insulated from said top and bottom surfaces, a plurality of said traces being disposed on said further surface.

14. The layout of claim 10 further including a further surface between said top and bottom surfaces insulated from said top and bottom surfaces, a plurality of said traces being disposed on said further surface.

15. The layout of claim 11 further including a further surface between said top and bottom surfaces insulated from said top and bottom surfaces, a plurality of said traces being disposed on said further surface.

16. The layout of claim 12 further including a further surface between said top and bottom surfaces insulated from said top and bottom surfaces, a plurality of said traces being disposed on said further surface.

17. The method of claim 1 wherein said substrate has at least first, second and third rows and first, second and third columns of said vias, a first trace of a first pair of said traces extending to a via in said first row of said first column closest to said chip and a second trace of said first pair of traces extending to a via in said second row of said first column and between said

first column and second column which is adjacent to said first column, a first trace of a second pair of said traces extending to a via in said first row of said second column closest to said chip and a second trace of said second pair of traces extending to a via in said second row of said second column and between said second column and third column which is adjacent to said second column, and a first and second traces of a third pair of said traces extending to vias in said third row of said first and second columns and disposed between said first and second columns.

18. The layout of claim 9 wherein said substrate has at least first, second and third rows and first, second and third columns of said vias, a first trace of a first pair of said traces extending to a via in said first row of said first column closest to said chip and a second trace of said first pair of traces extending to a via in said second row of said first column and between said first column and second column which is adjacent to said first column, a first trace of a second pair of said traces extending to a via in said first row of said second column closest to said chip and a second trace of said second pair of traces extending to a via in said second row of said second column and between said second column and third column which is adjacent to said second column, and a first and second traces of a third pair of said traces extending to vias in said third row of said first and second columns and disposed between said first and second columns.

ABSTRACT OF THE DISCLOSURE

A method of laying out traces for connection of bond pads of a semiconductor chip to a printed wiring board or the like and the layout. There is provided a substrate having top and bottom surfaces with a plurality of rows and columns of vias extending therethrough from the top surface to the bottom surface and having a solder ball secured at the bottom surface to each via. A plurality of pairs of traces is provided on the top surface, each trace of each pair of traces extending to a different one of the vias and extending to vias on a plurality of the rows and columns, each of the traces of each pair being spaced from the other trace by up to the diameter of the solder ball, being maximized for identity in length and being maximized for parallelism. Each of the traces of a pair is preferably be further maximized for identity in geometry. A differential signal pair is preferably applied to at least one of a pair of traces. The layout can further include a further surface between the top and bottom surfaces insulated from the top and bottom surfaces, a plurality of the traces being disposed on the further surface.

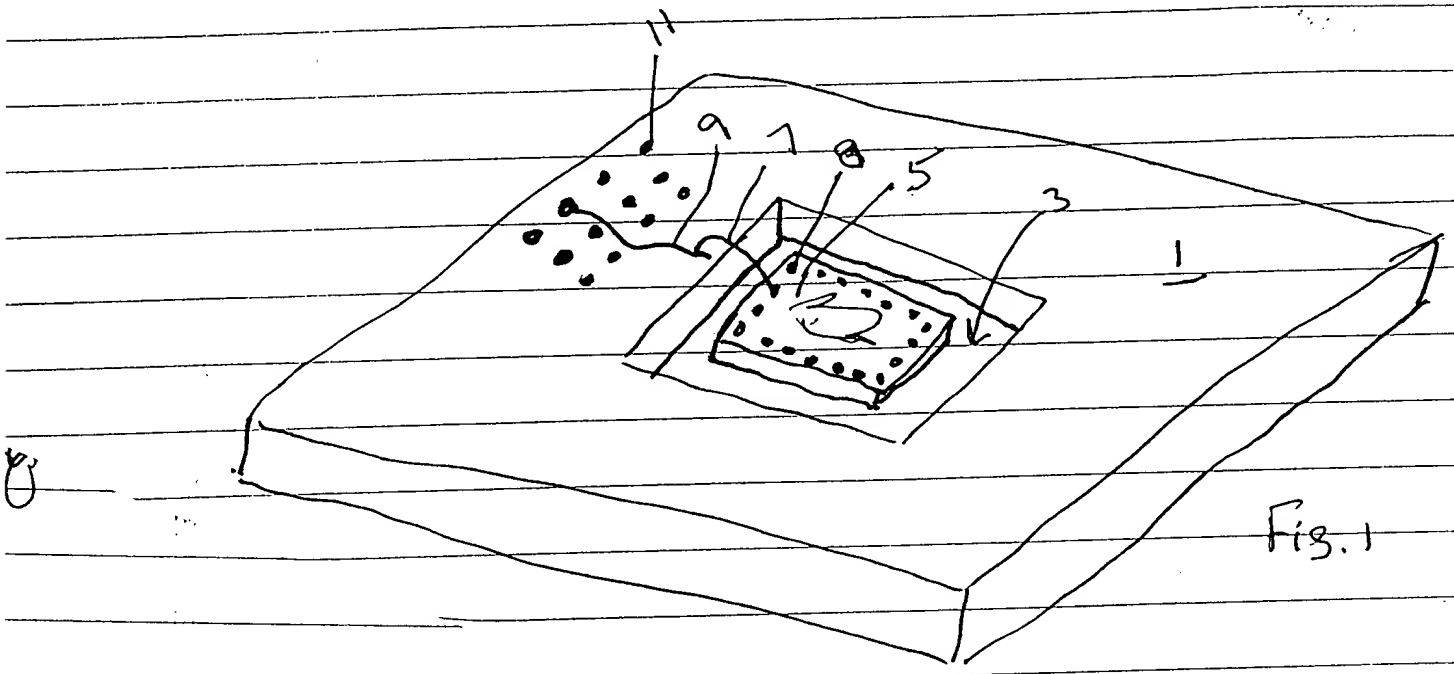

Fig. 1

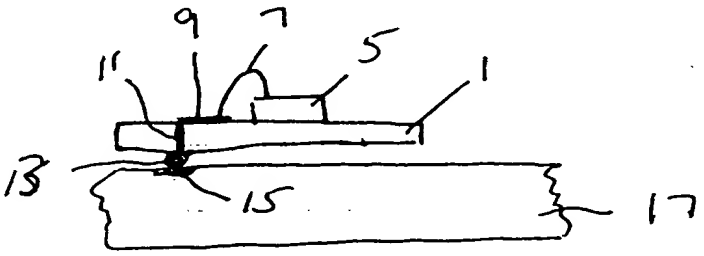

Fig. 2

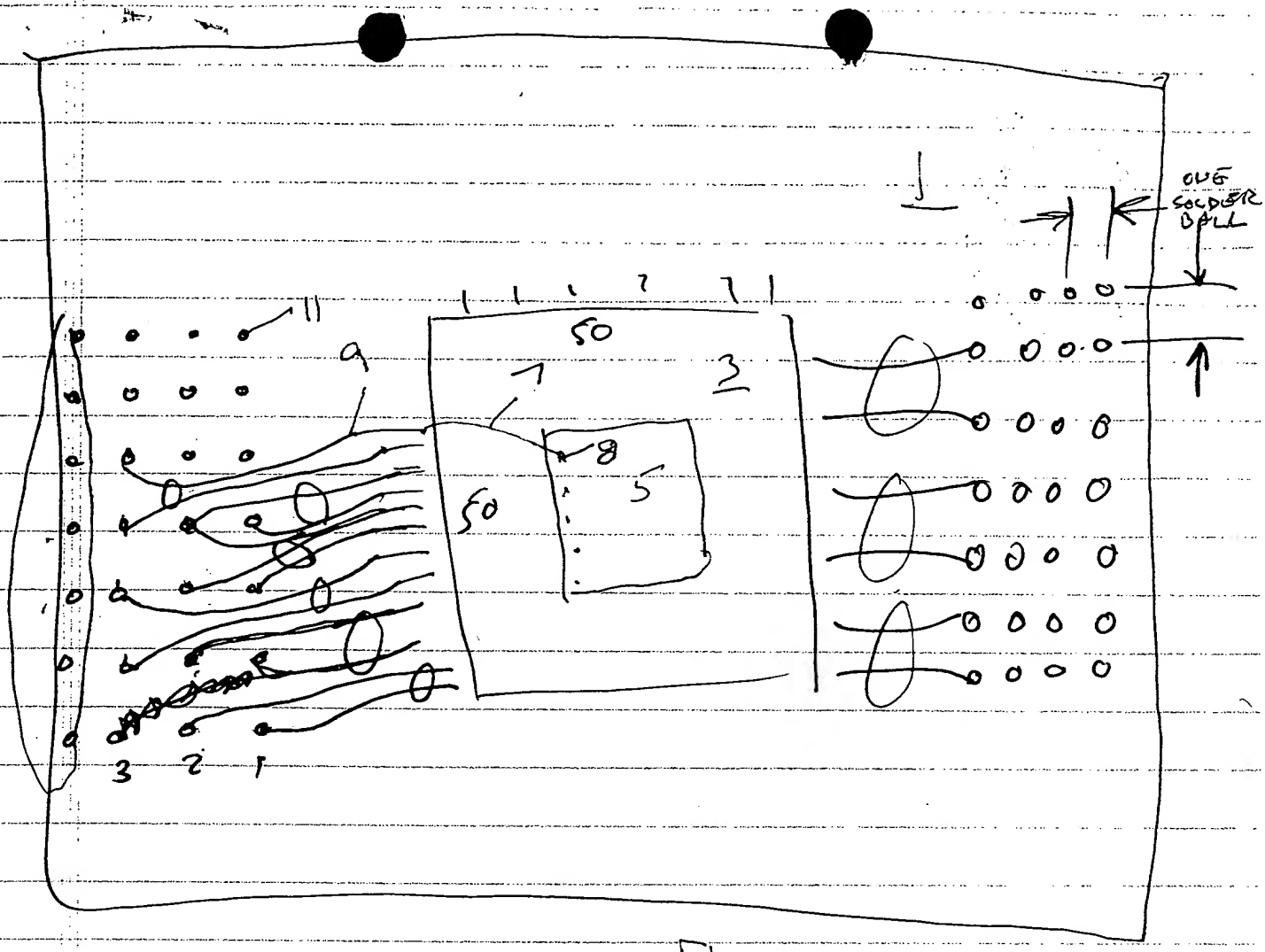

Fig. 3

Pairs: - Adjacent
- parallel
- equal Length (within one ball Pitch)

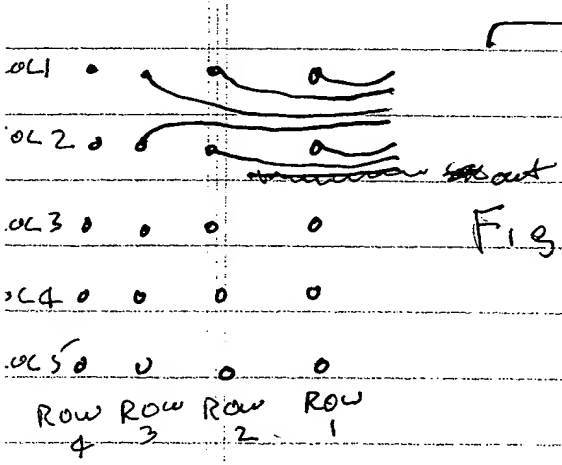

Fig. 4